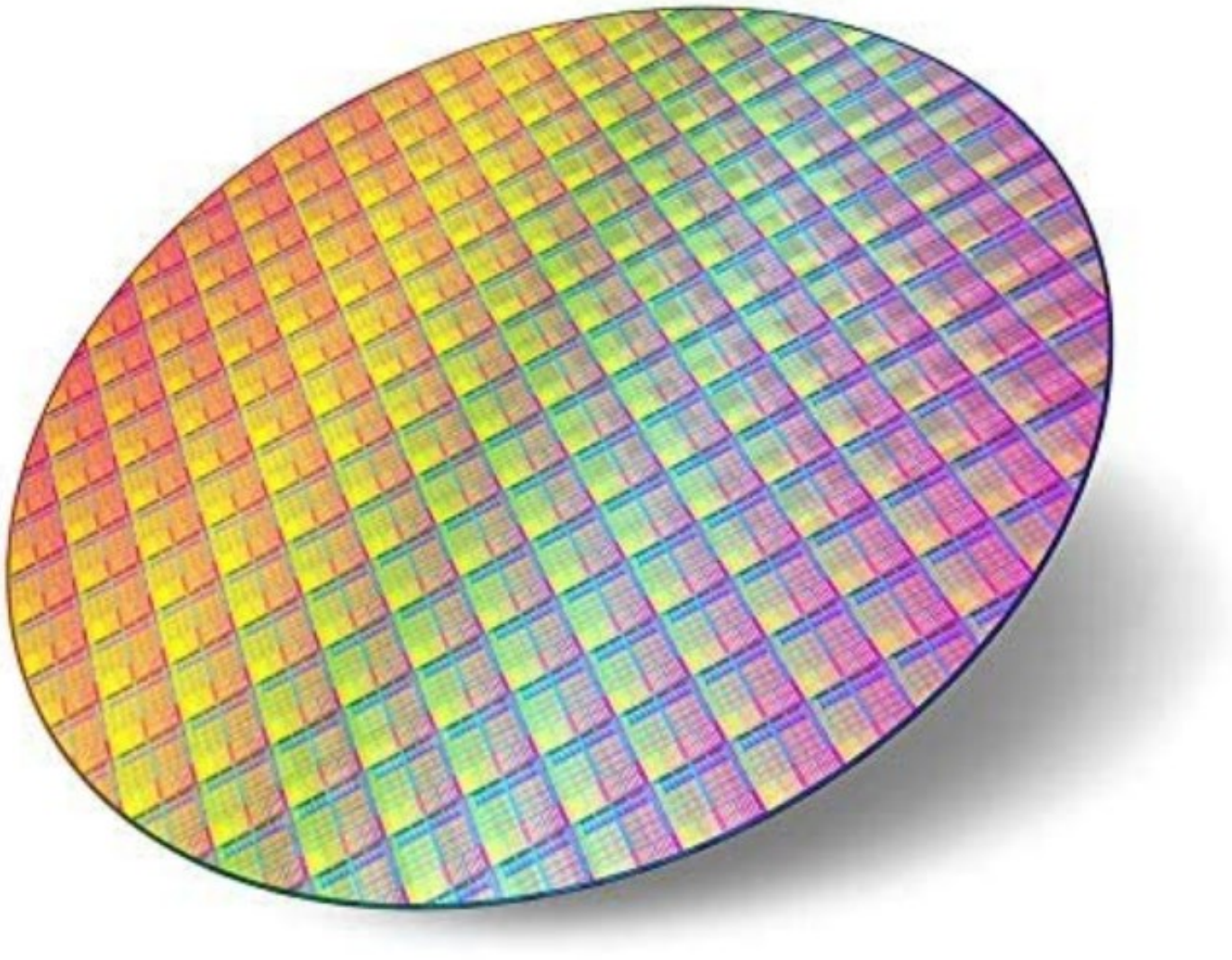
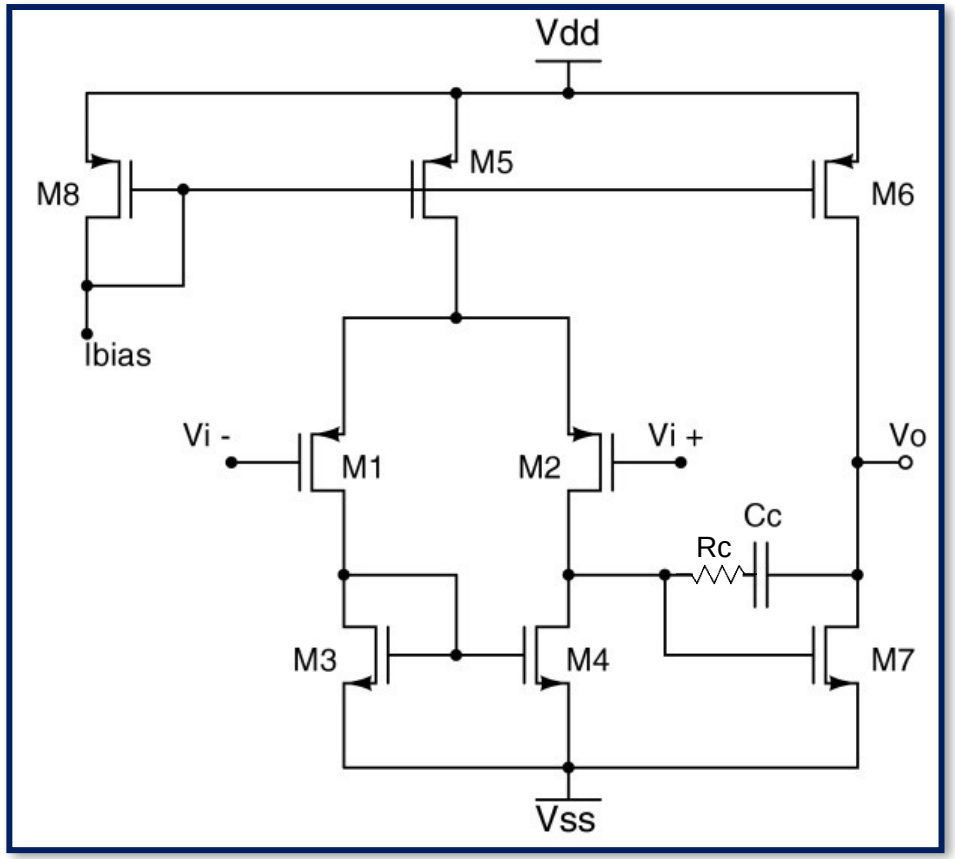
Analog IC Design Under Constraints

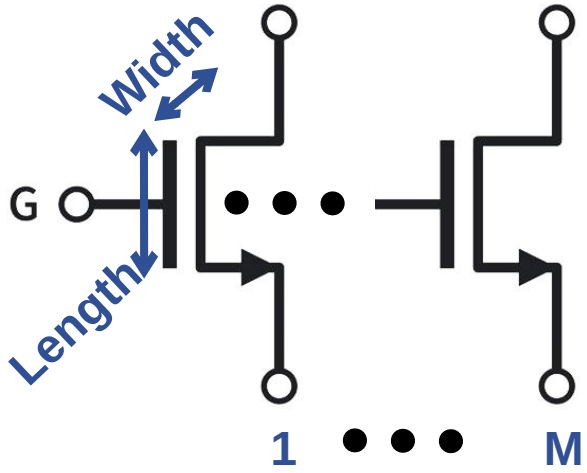


Nicolai Dahl

DTU Chip Day
April 14th 2026

Analog Circuit Sizing

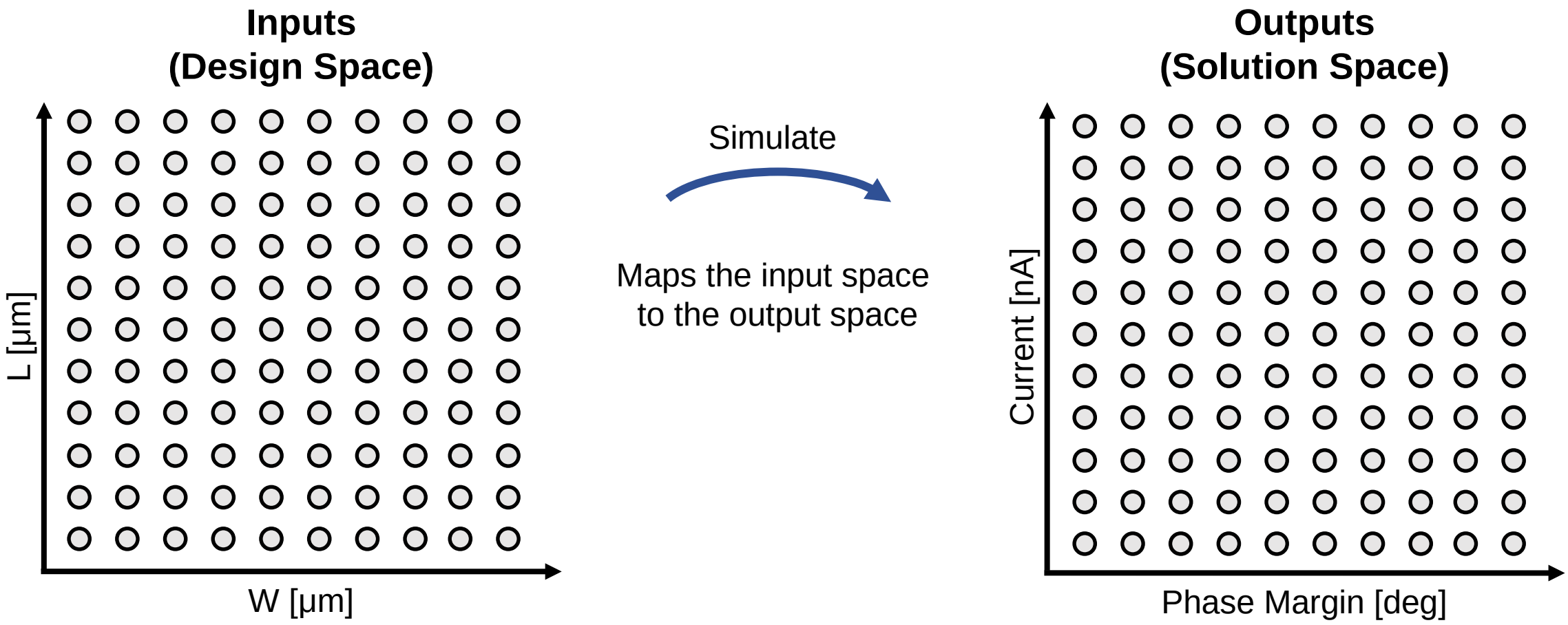




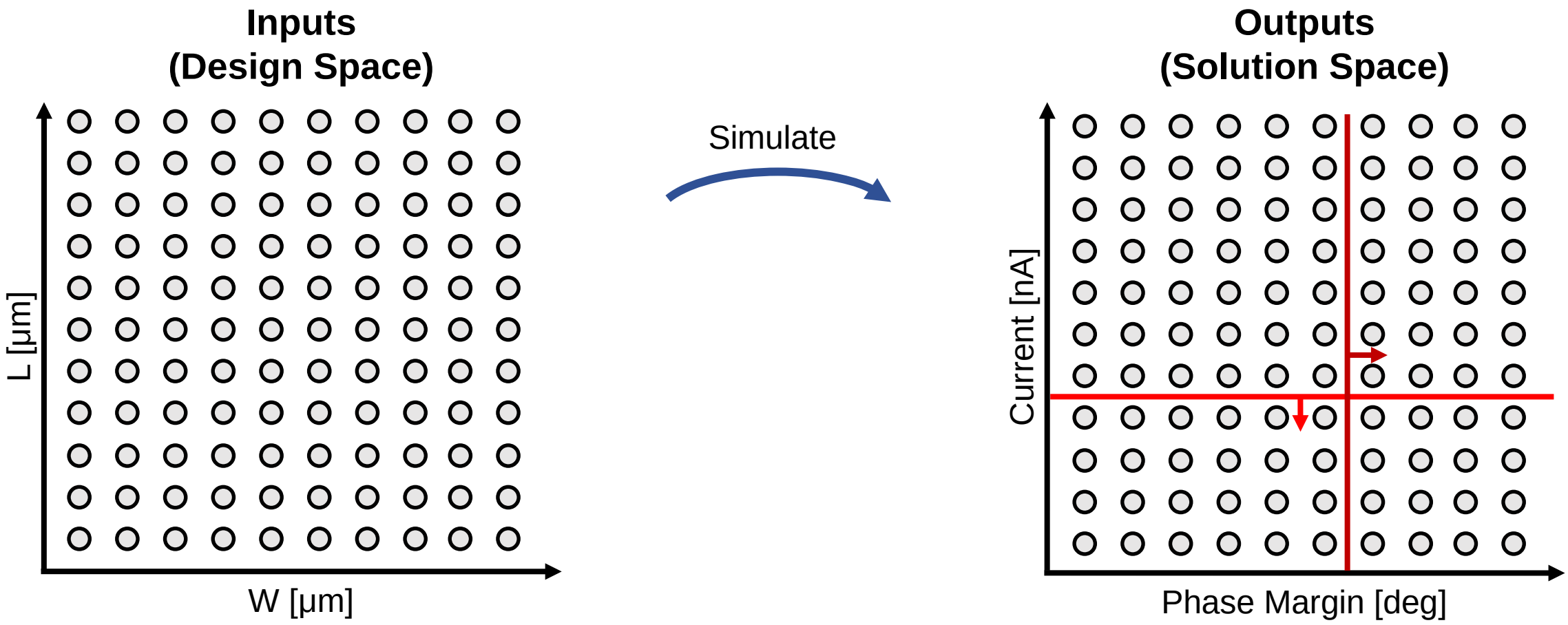
Adjust transistor sizes to:

- Minimize Power or Area
- Satisfy all Specifications
- Increase Robustness

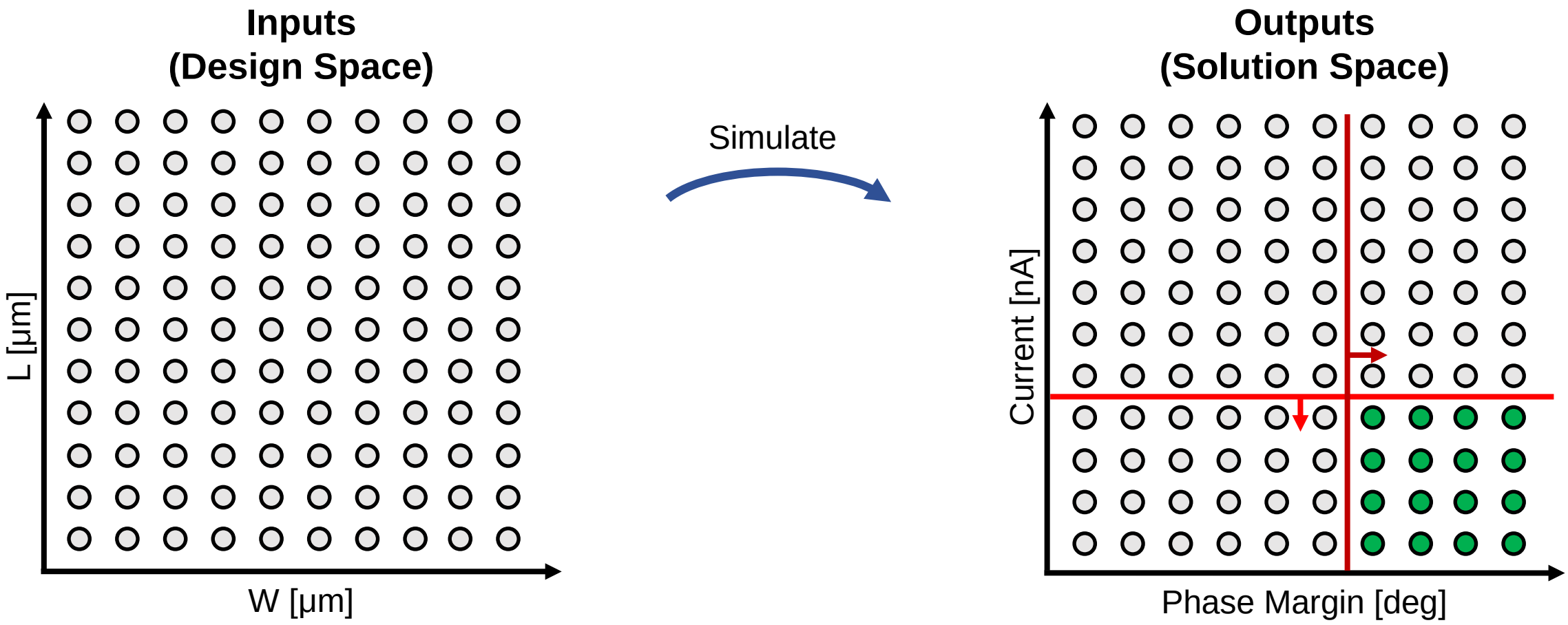
A Toy Example



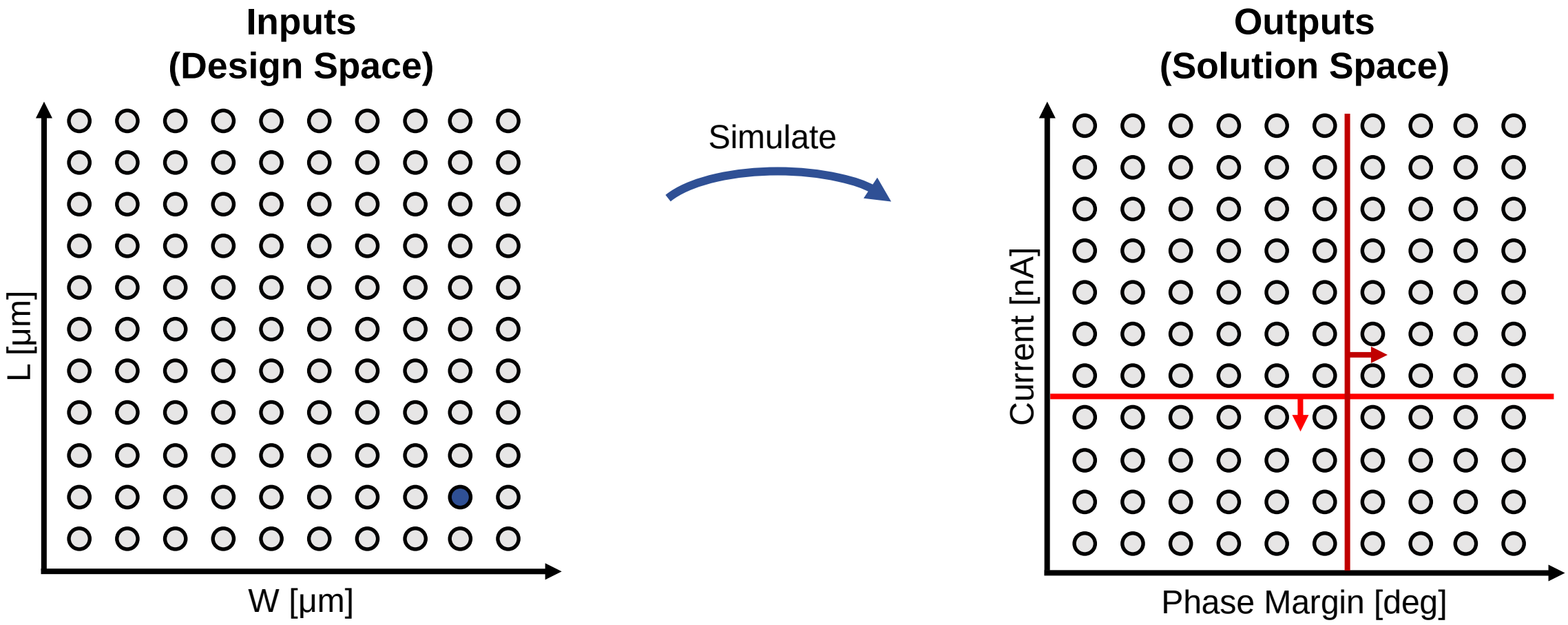
Adding Specifications



Target Region



We can simulate a point…



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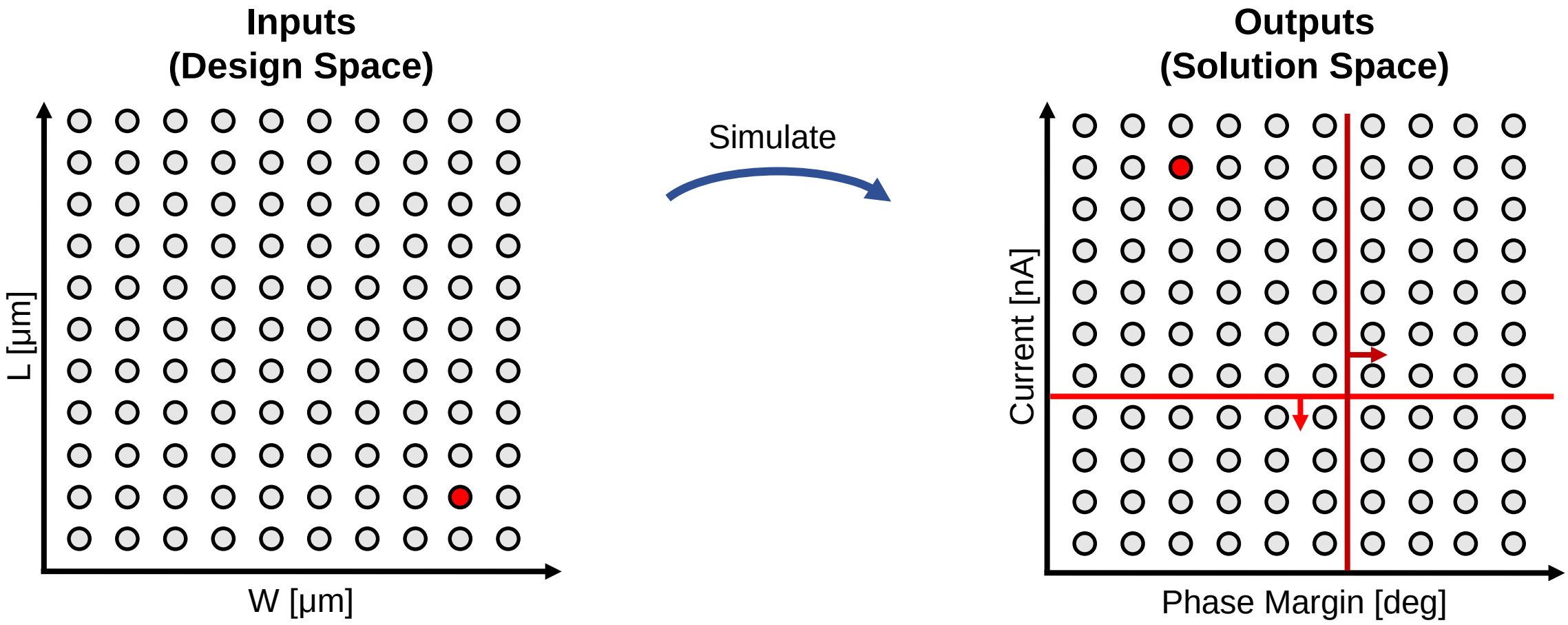
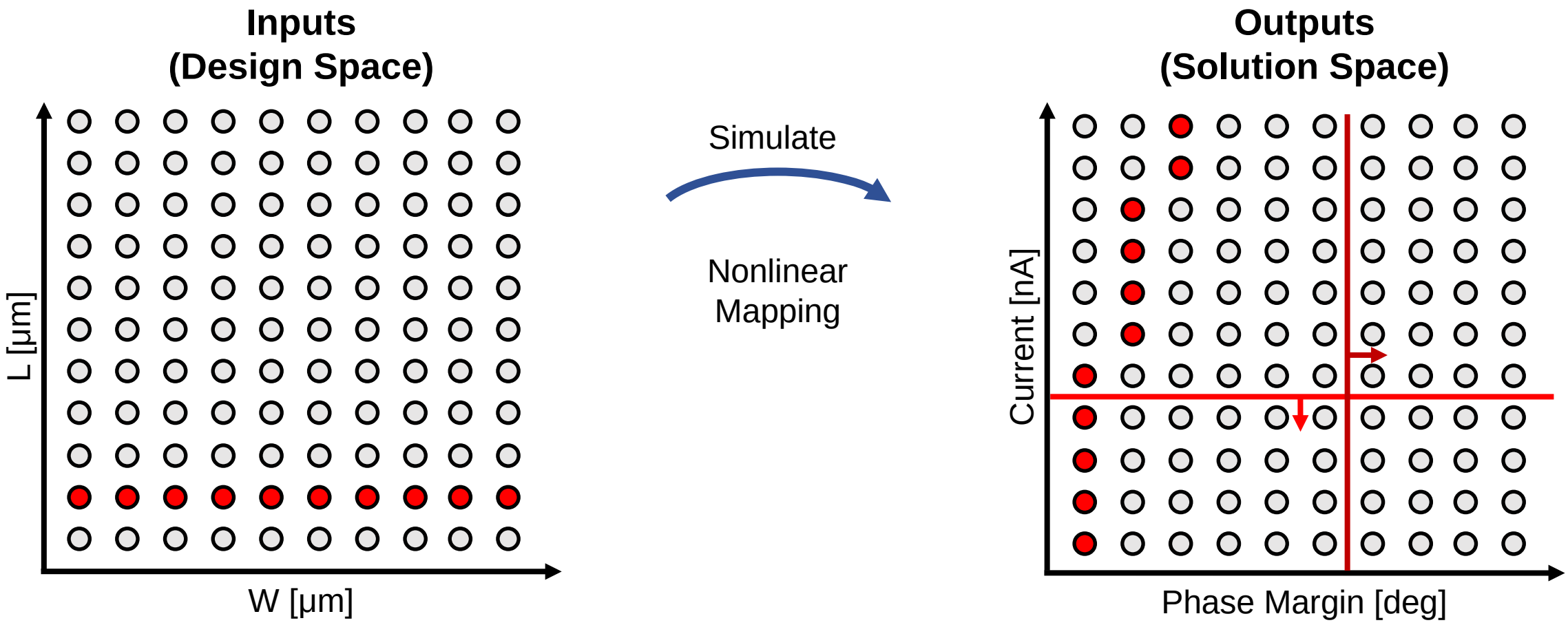
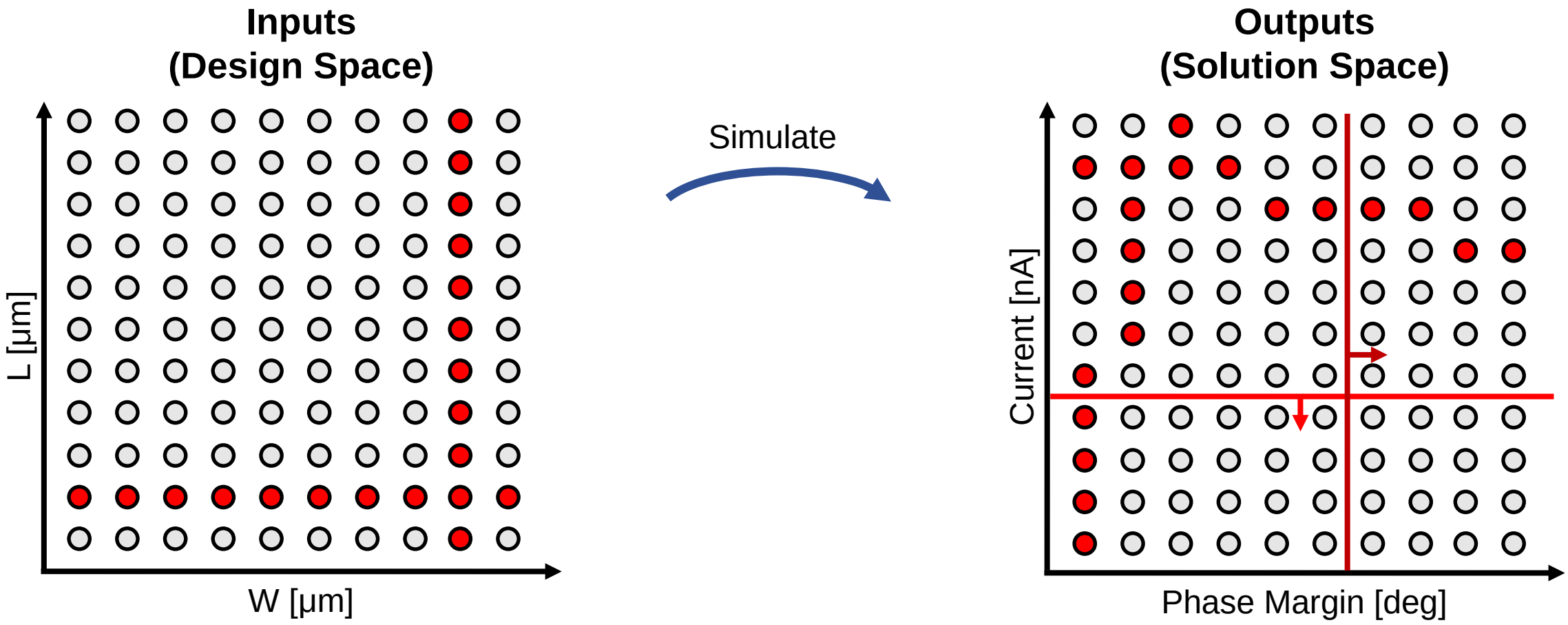


…or do a sweep

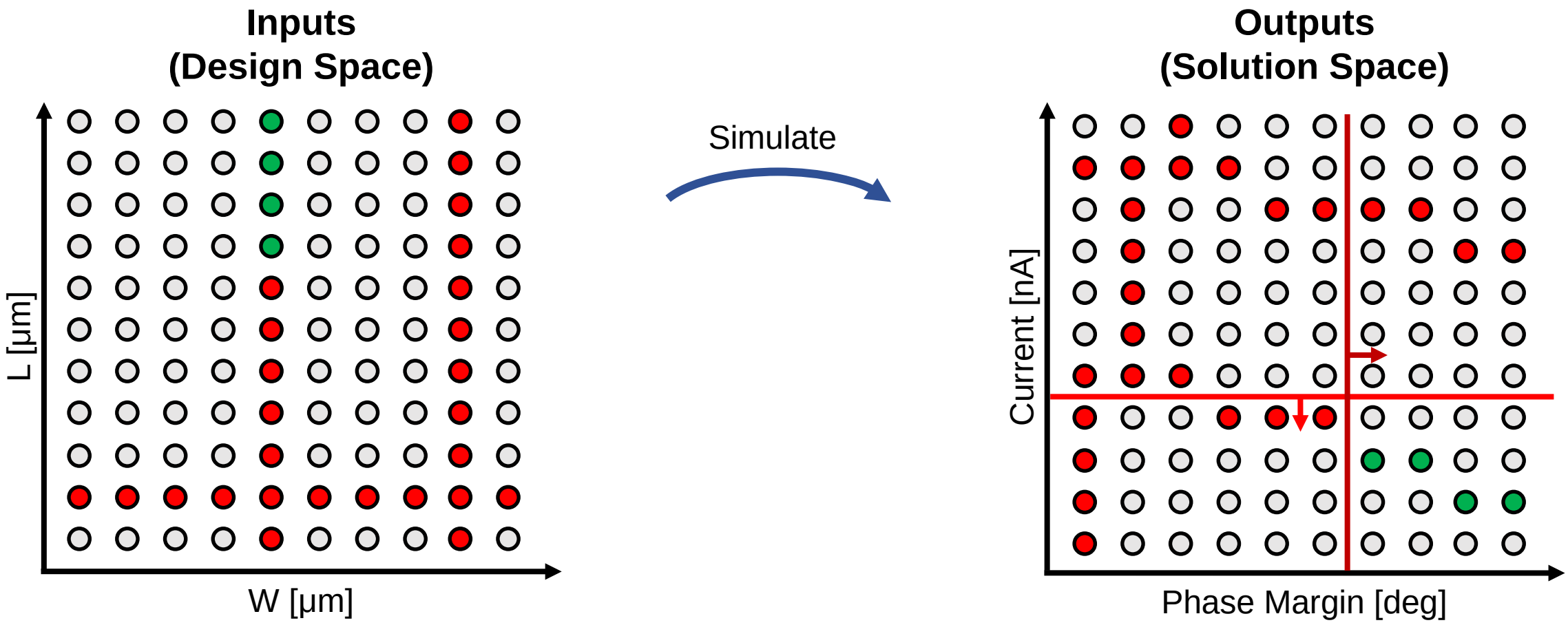

Inputs
(Design Space)
L [µm]
W [µm]
Simulate
Nonlinear
Mapping
Outputs
(Solution Space)
Current [nA]
Phase Margin [deg]

Sweep, Think, and Repeat

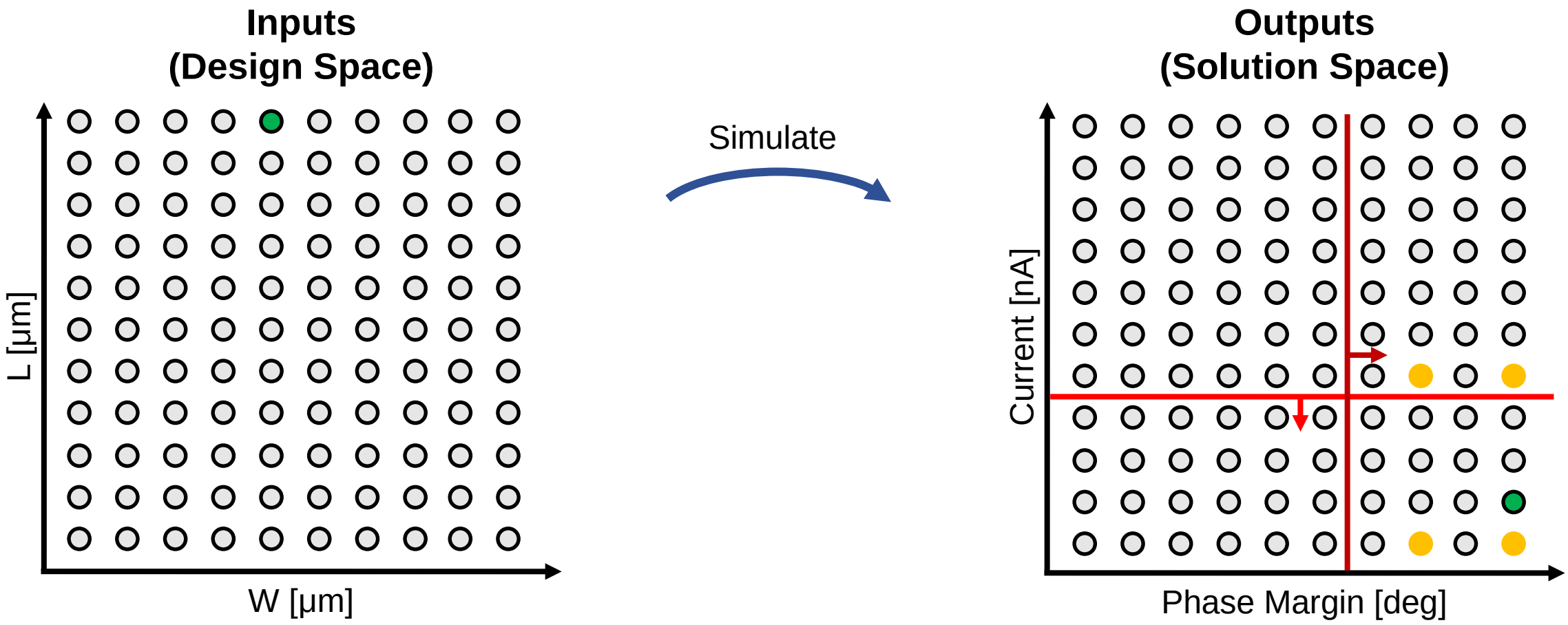
…And sometimes a bit of *Gut Feeling*



…Until we find a solution



Finally check Corners and MC

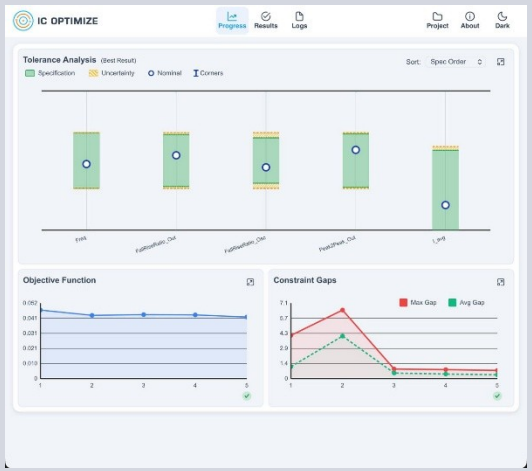


The Curse of Dimensionality

- As the number of inputs and outputs grow, the spaces grows exponentially!!
- The same happens when you run MC or add Corners
- This is what makes Analog IC Design truly challenging

This can be done more efficient!

Our Solution - OPUS



IC OPTIMIZE
AMS Device Sizing

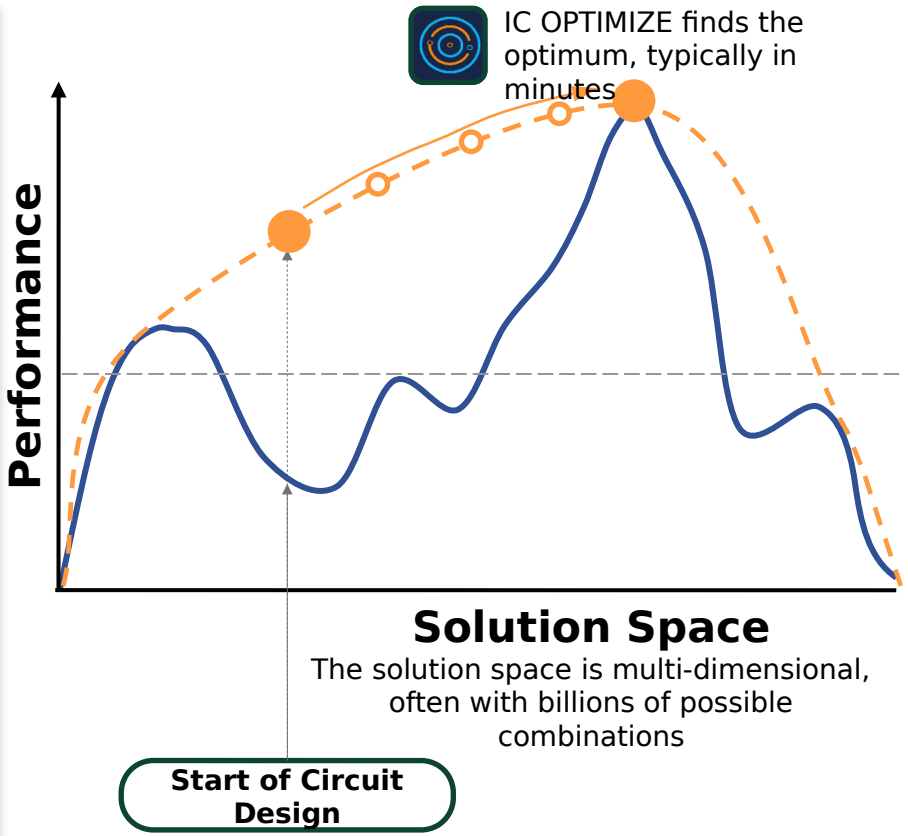
IC OPTIMIZE has developed an **Optimization Engine** that employs **Convex Relaxation Techniques** to reach a design with the minimum number of simulations.

Circuit Schematic & PDK

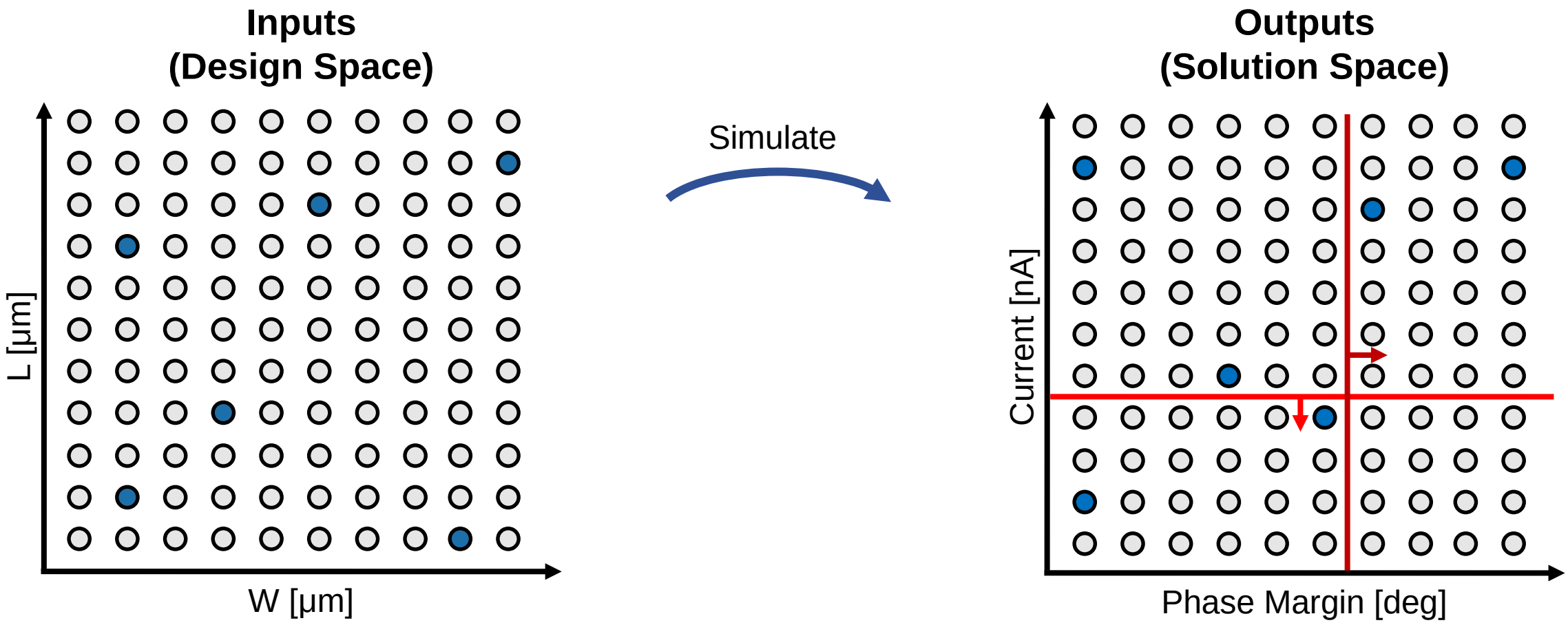
Specifications

Layout Ready Circuit with OPTIMAL DEVICE SIZING

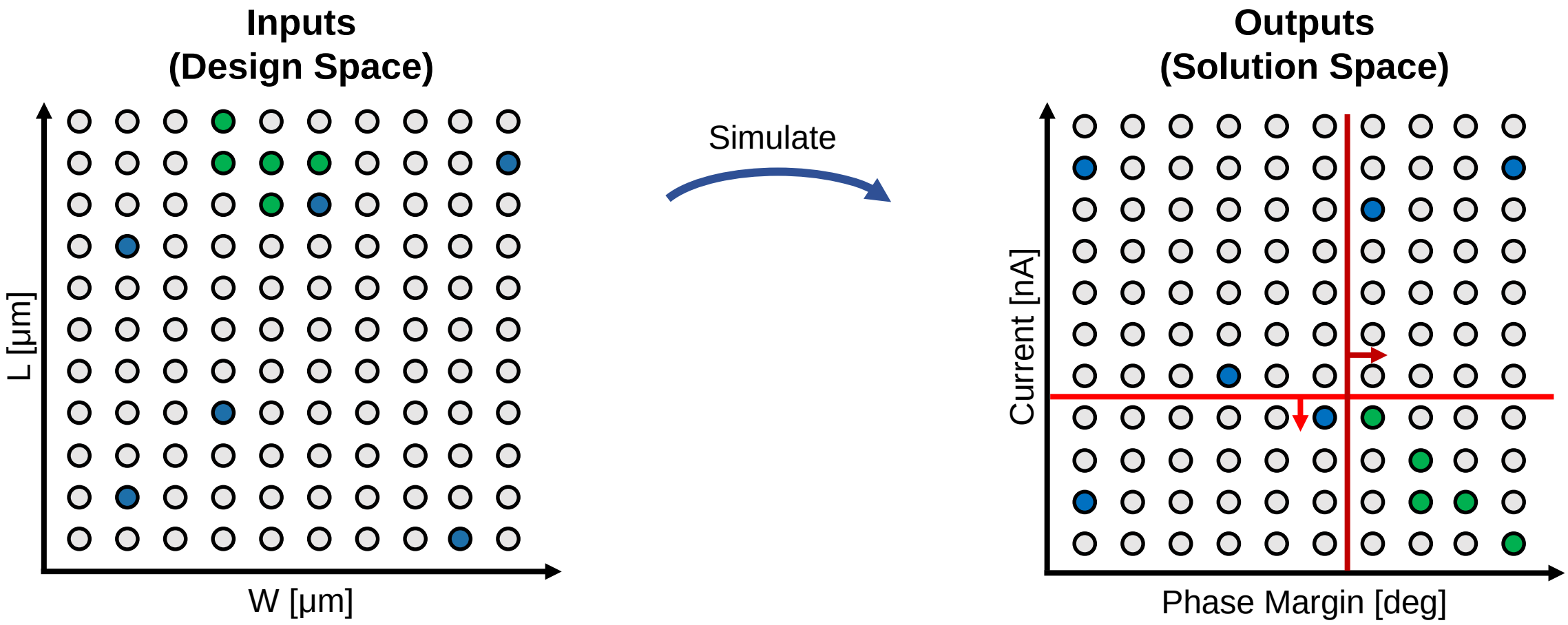
Existing State-of-the-art EDA Tool Suite



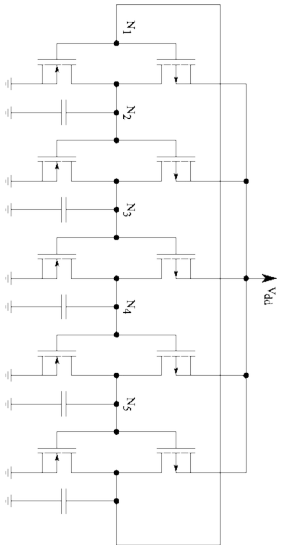
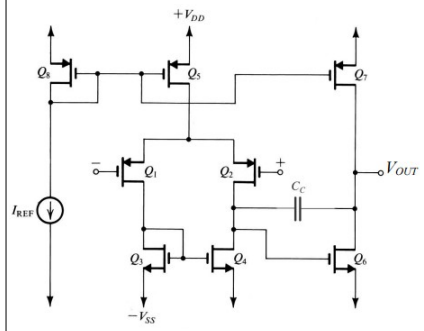
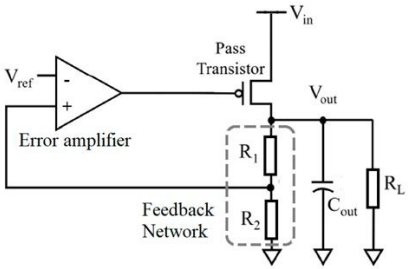
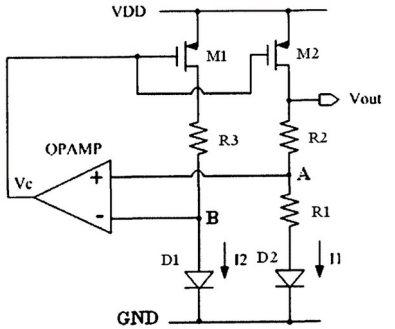
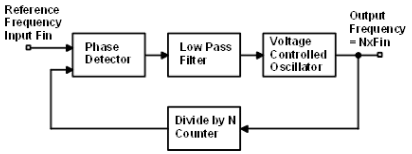
Step 1: Samples the design space



Step 2: Optimize on the learned mapping



Performance

Circuit	Ring Oscillator	Op-Amp	LDO (Low-Dropout Regulator)	Bandgap Reference	PLL (Phase-Locked Loop)
Schematic					
Variables	9	10	13	17	17
Search space	3e11	2e10	3e12	1e22	2e22
Specifications	5	8	10	10	10
Needed simulations OPUS	34	42	44	169	122

Q & A