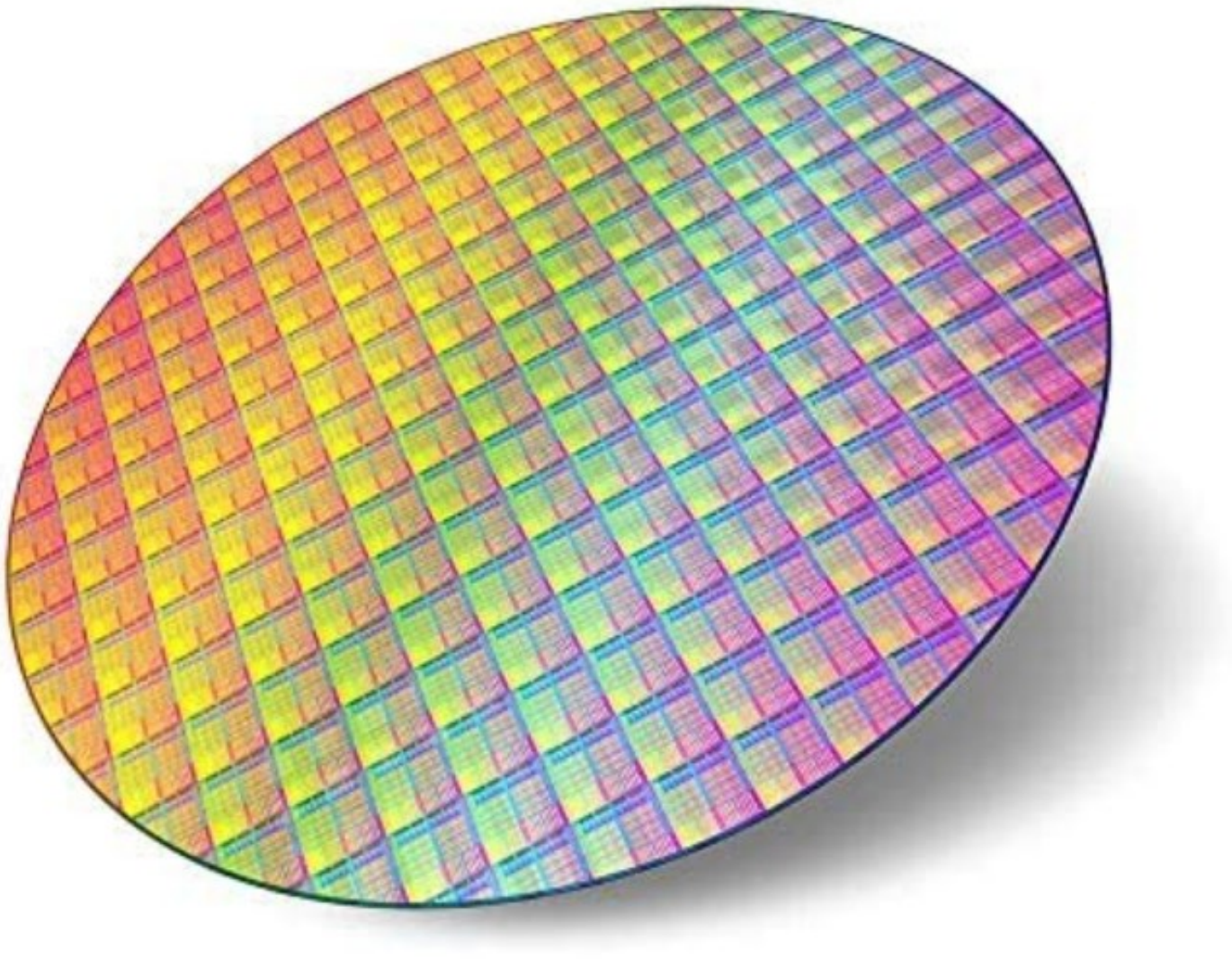
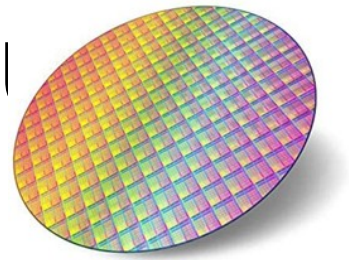
First Student Tape-Out



Martin Schoeberl

DTU Chip Day
April 14th 2026

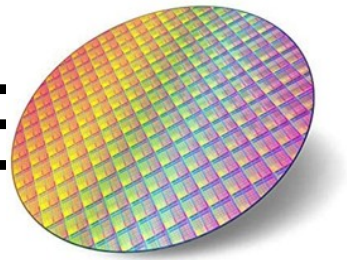
Motivation: A new BSc in Computer Engineering



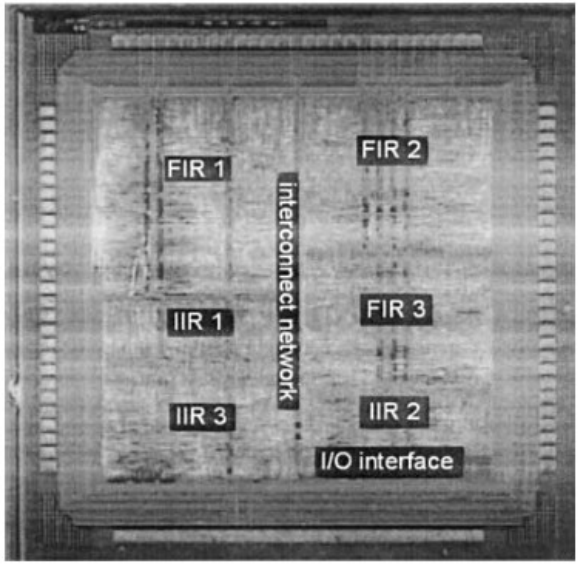
- We need more chip designers!

  => DTU Chip Day ;-)
- We have a BSc degree in Computer Engineering
  - Started fall 2023
  - With a specialization in chip design
- We use open-source tools only
  - Install tools locally
  - Do your chip design on your laptop (including hardening)
    - Local from RTL to GDSII
- Bring real chip tape-out into the BSc education of CE and EE

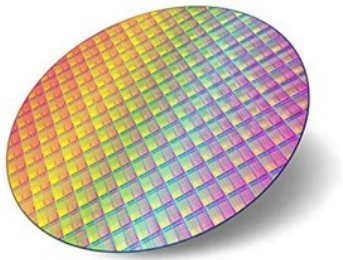
Last Chip at DTU Compute (ESE



- Fabricated 2001/2002
  - Paker, O., Sparsø, J., Isager, M., Haandbæk, N. & Nielsen, L. S.,
    A Low-Power Heterogeneous Multiprocessor Architecture for Audio Signal Processing
    Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology. 37, 1, p. 95-110, 2004
- A PhD project of Özgün Paker
- Supervisor Jens Sparsø
- Partly funded by Oticon
- Not a BSc or MSc student project!

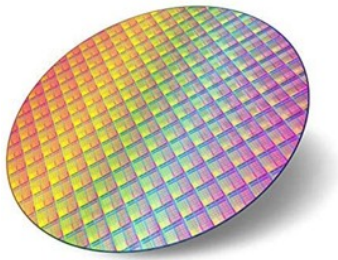


Tape-Out for Education

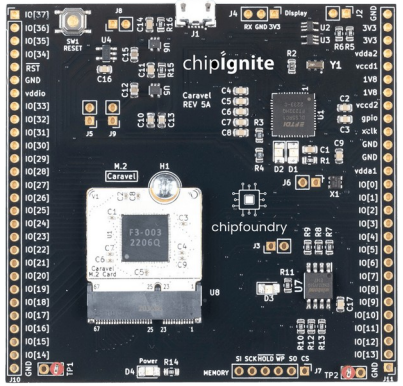


- First (educational) student tape-out at DTU Compute
  - Expose students in the last semester of BSc to a real tape-out
  - In an introduction to chip design course
- Open-source is an enabler
  - Work on your laptop in a cafe/train/airplane
  - If you can run it locally, you might use it more often
- Old technology and multi-project wafer (MPW) are enablers
  - Low-cost tape-out
- Tjark and I did a test chip as preparation last fall

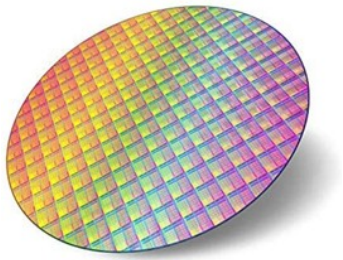
SkyWater 130 nm



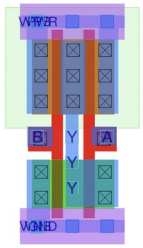
- SkyWater was formerly Cypress
  - Cypress made fast SRAMs
- Opened up their 130 nm process in 2020
  - SkyWater, Google, and Efabless
  - Now, chipfoundry is doing the MPW
- 10 mm2 space
- 100 packaged dies for $ 15000
  - Plus test board
- We reserved a slot, tape-out deadline 13th May
- Also used by Tiny Tapeout



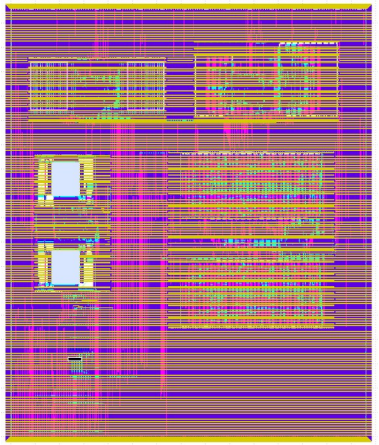
All in Open Source



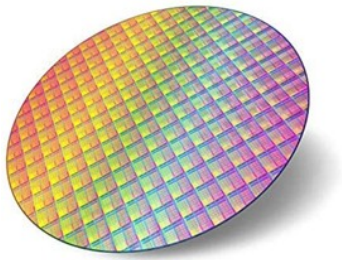
- Tools (LibreLane)
- PDK for SkyWater130
  - We can explore the detai



- Teaching material
  - Slides: https://github.com/os-chip-design/chip-design-intro
  - Booklet: https://github.com/os-chip-design/chip-desi
- Student project
  - https://github.com/os-chip-design/dtu-soc-2026
- We are allowed to publish the final GDS

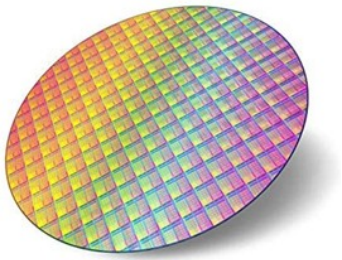


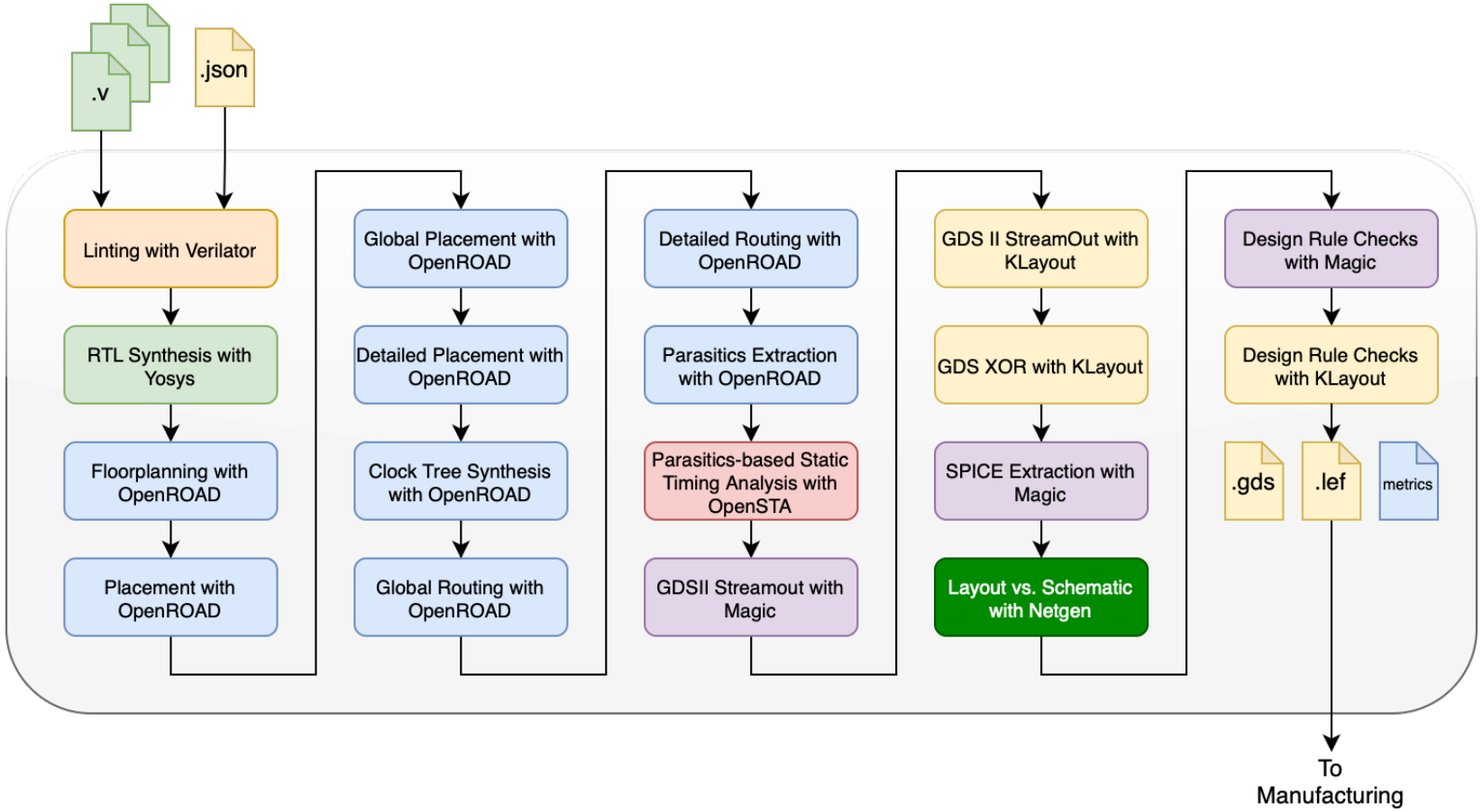
LibreLane ASIC Design Flow



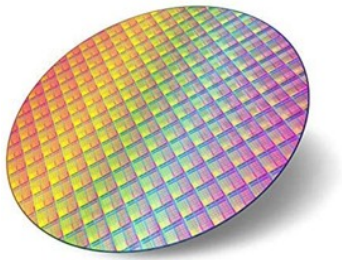
- LibreLane is an open-source toolchain for ASIC design
  - Automates the process from RTL to GDSII for tapeout
  - Ensures manufacturability with verification steps
  - Uses open-source tools (e.g., Yosys, OpenROAD, and Magic)
- Install locally
  - Linux and MacOS (also ARM version!)
- Former OpenLane 2, former OpenLane

LibreLane Design Flow

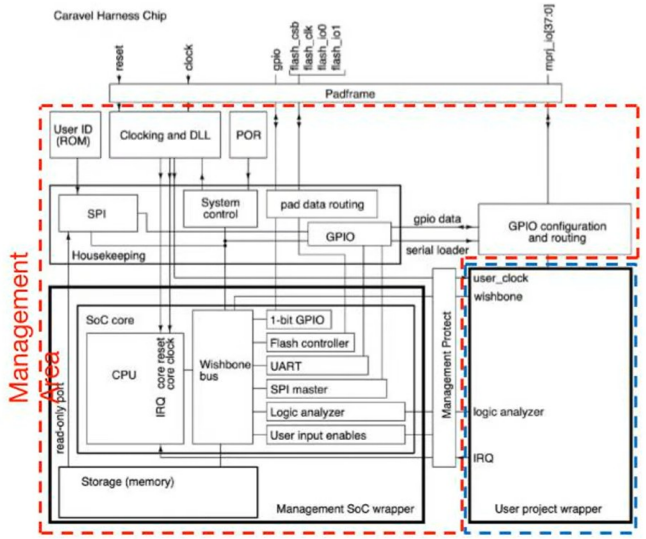


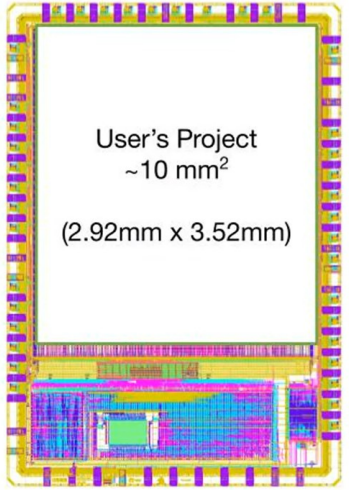


Caravel Framework

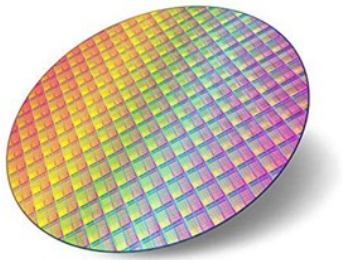


- Framework for chip design from efabless
  - Now chipfoundry
- Management area provided
  - RISC-V core
  - SPI for Flash
  - UART
- Padframe and GPIO
- 10 mm2 user area
- Wishbone interface to the user project



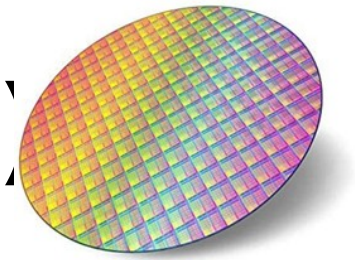


Status



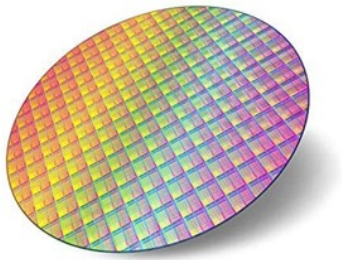
- Integrated a RISC-V processor (Wildcat)
- Added a VGA controller for a terminal
- Fighting with memory
  - Working on boot options
- 10 mm2 is a lot of space
  - We might do a multicore
  - We have space for additional projects
  - Do you want to add your project?
- I am a bit stressed if we can make it for the deadline
- Tape-out sponsored by Edu4Chip

Main Learning Outcome (So far)

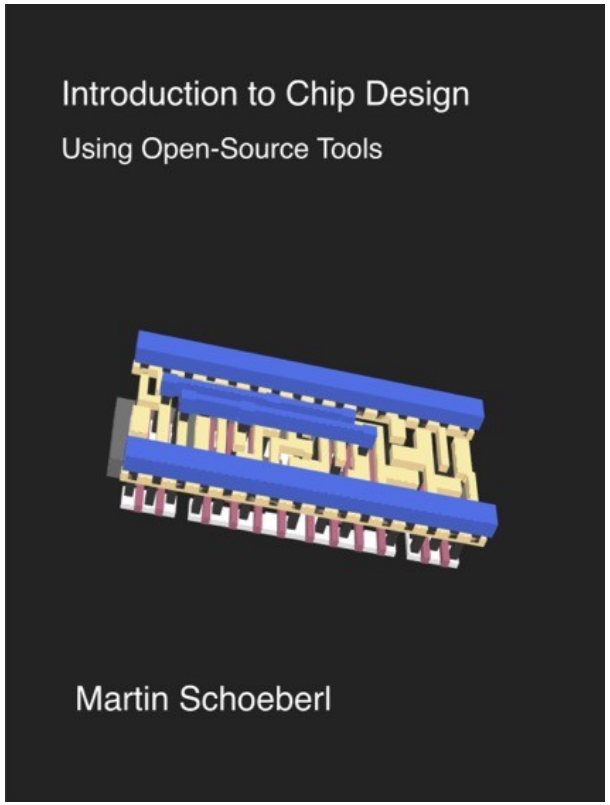


- Memories are a pain
  - We are used to Verilog/Chisel-coded memories in FPGAs
- Working on a common repo leads to conflicts
  - Need to learn best practices with git
- Continuous integration is key
  - Integration of sub-projects as early as possible
    - Avoid git branches
  - GitHub actions build the chip and run tests

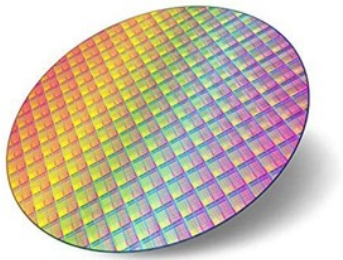
Future Work



- Started an open-source textbook
- Maybe our own framework
  - Instead of Caravel
- Maybe a DTU microcontroller
  - To be used in teaching
- We are part of a Chips-JU project
  - ODE4EC
  - On open-source EDA tools
  - Two PhD positions open



Summary



- First student tape-out at DTU Compute
- Project-oriented chip design course
- Open-source only
  - From tools to teaching material to RTL to G
  - No server needed (except GitHub)
- Tape-out very soon
- Some feedback from students:
  - *The course is fun and cool*
  - *The coolest course I've had so far*